REMARKS

Applicants appreciate the thorough examination of the present application as evidenced by the Final Action. However, Applicants request withdrawal of the rejections for at least the reasons discussed below.

Interview Summary:

Applicants' undersigned representative appreciates the courtesy extended by the Examiner during the telephonic interview of March 29, 2007. During that interview, both the Section 102 and 112 rejections were discussed. Agreement was reached that, subject to any issues that may be raised by a subsequent search, the rejections would be overcome by amending the independent claims as needed to make clear what connections are provided with no synchronizing "therebetween."

The Section 112 and 102 Rejections:

Claims 1-24 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. Final Action, p. 4. Claims 1-24 stand rejected under 35 U.S.C. § 102(b) as anticipated by United States Patent No. 5,774,476 to Pressly *et al.* ("Pressly"). Final Action, p. 5. As noted above, during the interview agreement was reached that the rejections appear to be overcome in light of Applicants' clarification of the "without synchronizing" recitations. To expedite review by the Examiner, Applicants provide the following comments regarding the same for the respective independent claims.

Independent Claims 1 and 4:

Independent Claims 1 and 4 have been amended to replace "therebetween" with "between the MUX unit and the core block or between the MUX unit and the input side sub logic circuit." In contrast, as seen in Figures 1-3 of Pressly, flip-flops coupled to a clock signal synchronize the communication of data between the customer-specified logic 12 and the embedded core 14 with a clock. Accordingly, independent Claims 1 and 4 and

the claims that depend therefrom are patentable for at least these reasons.

Independent Claims 13-16 and 20-21:

Independent Claim 13 recites " without synchronizing the output data between the output ports of the core block and the MUX unit." Such is illustrated, for example, in replacement Figure 5, where the output data C2D1 through C2DN are provided from the core block 530 to the MUX unit 520 and selectively from the MUX unit 520 to inputs of the core block 530 without synchronizing to a clock in either connection between the core block and the MUX. In contrast, as seen in Figures 1-3 of Pressly, flip-flops coupled to a clock signal synchronize the communication of data between the customer-specified logic 12 and the embedded core 14 with a clock, including in the routing of outputs of the core 14 fed back into the core 14. Claim 14 includes similar recitations. Independent Claims 15-16 and 20-21 have been amended to include corresponding recitations. Accordingly, independent Claims 13-14 and 20-21 and the claims that depend therefrom are patentable for at least these reasons.

CONCLUSION

Applicants respectfully submit that the reference cited in the present rejections does not disclose or suggest the present invention as claimed and that the written description requirement is met for the reasons set out above and as discussed during the Interview. Accordingly, Applicants respectfully request reconsideration of the rejections by the Examiner and allowance of all the pending claims and passing this application to issue.

Respectfully submitted,

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CERTIFICATION OF TRANSMISSION

I hereby certify that this correspondence is being transmitted via the Office electronic filing system in accordance with § 1.6(a)(4) to the U.S. Patent and Trademark Office on April 5, 2007.

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